REMARKS

Claims 1 – 20 are pending in the application. Claims 11,13, and 14 have been amended. Claims 1-10 have been allowed, and Claims 16-20 have been withdrawn pursuant to a restriction requirement. No new matter has been introduced by the amendment.

RESTRICTION REQUIREMENT

In the applicant's previous response of September 23, 2005, the applicants set forth grounds for traversing the pending restriction requirement. In particular the applicants pointed out that the hypothetical process set forth in the Office Action of August 23, 2005, failed to justify the restriction requirement. In particular, the Office Action stated "(i)n the instant case, the semiconductor device can be fabricated with a conductive material other than polysilicon." The applicants point out that method Claim 11 recites the step of providing a polysilicon layer. Correspondingly, device Claim 16 recites a polysilicon layer. Accordingly, Claims 11 and 16 each recite a particular semiconductor material. Accordingly, the applicants respectively request reconsideration and withdrawal of the restriction requirement.

Should the Restriction Requirement be withdrawn, the applicants prepare to amend claims 16-20 in a manner corresponding to the amendment of claims 11, 13, and 14 set forth herein. The applicant's proposed amendment of the withdrawn claims is attached hereto as Attachment A.

Claim Objections

"An objection has been set forth to Claim 11 regarding the recitation of providing an undoped polysilicon layer over said undoped portion of said polysilicon layer."

This objection is overcome in view of the amendment of Claim 11, such that Claim 11 now recites that the undoped polysilicon layer is provided over said in-doped portion of said polysilicon layer.

Rejection Under 35 U.S.C.§ 102 (b)

Claims 11 and 15 have been rejected over Cheek et al. This rejection is overcome in view of the amendment of Claim 11 together with following remarks.

Claim 11, as amended, recites a method that includes providing a polysilicon layer having an undoped portion to form a gate of a p-MOS transistor and a n-doped portion to form a gate of an n-MOS transistor. Claim 11 further recites providing an n-doped polysilicon layer over said un-doped portion of said polysilicon layer and providing an un-doped polyilicon layer over said n-type doped portion of said polysilicon layer. The applicants respectively assert that the method recited in Claim 11 distinguishes over Cheek et al. In particular, Claim 11 has been amended to expressly recite that the doped layers contain only one type of doping, namely, n-type doping. Accordingly, Claim 11 has been amended to satisfy the requirements for patentablility as set forth in the Examiner's statement of reasons for allowance in paragraph 17 of the instant Office Action.

Claim 15 depends from Claim 11 and is allowable in view of the amendment and remarks pertaining to Claim 11.

Rejection Under 35 U.S.C. § 103 (a)

Claim 12 has been rejected over Cheeks et al. in view of Gardner et al. This rejection is overcome in view of the amendment and forgoing remarks pertaining to Claim 12.

Claim 13 has been rejected over Cheek et al. and Wolf, Silicon Processing for the VLSI Era, Lattice Press (2002). This rejection is overcome in view of the amendment of Claims 11 and 13 together with following remarks.

Claim 13 depends from Claim 11 and recites the further step of providing a bottom anti-reflective coating over said n-doped polysilicon layer and said undoped polysilicon layer. Accordinly, Claim 11 has been amended to correspond to the amendment of Claim 11. Claim 13 is allowable in view of the amendment and foregoing remarks pertaining to Claim 11.

Claim 14 has been rejected over Cheek et al. and Callister, Material, Science, and Engineering, 4th edition, John Wiley and Sons in (1997). This rejection is overcome in view of the amendment of Claims 11 and 14 together with following remarks.

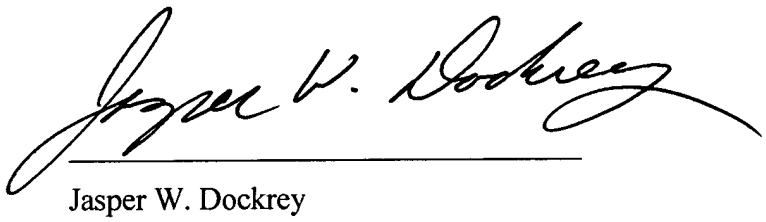
Claim 14 has been amended to correspond to the amendment of Claim 11 and recites that the step of providing said n-doped polysilicon layer over said undoped portion of said polysilicon layer comprises doping said polysilicon layer over said undoped portion with approximately equal doping to said n-doped portions of said polysilicon layer. Accordingly, Claim 14 has been amended to correspond with the amendment of Claim 11. Claim 14 is allowable in view of the amendment remarks pertaining to Claim 11.

Allowable Subject Matter

The applicants acknowledge the allowance of Claims 1-10 with appreciation.

The applicants have made a novel and non-obvious contribution to the art of semiconductor device fabrication. The claims that issue distinguish over the cited references and are in condition for allowance. Accordingly, such allowance is now earnestly requested.

Respectfully submitted,



Jasper W. Dockrey
Registration No. 33,868
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

ATTACHMENT A

16. (withdrawn - currently amended) An integrated circuit having a p-MOS transistor and an p-MOS transistor, said integrated circuit comprising:

a gate oxide layer on a substrate;

polysilicon layer having an undoped portion to form a gate of a p-MOS transistor and a n-doped ~~doped~~ portion to form a gate of an n-MOS transistor;

a n-doped ~~doped~~ polysilicon layer over said undoped portion of said polysilicon layer; and

an undoped polysilicon layer over said n-doped ~~undoped~~ portion of said polysilicon layer.

17. (withdrawn) The integrated circuit of claim 16 further comprising a hard mask layer provided over said polysilicon layer.

18. (withdrawn - currently amended) The integrated circuit of claim 16 further comprising a [[a]] bottom antireflective coating over said n-doped ~~doped~~ polysilicon layer and said undoped polysilicon layer.

19. (withdrawn - currently amended) The integrated circuit of claim 16 wherein said n-doped ~~doped~~ polysilicon layer over said undoped portion of said polysilicon layer comprises a doped polysilicon layer with approximately equal doping to said n-doped ~~doped~~ portion of said polysilicon layer.

20. (withdrawn) The integrated circuit of claim 16 further comprising a gate of said p-MOS transistor and a gate of said n-MOS transistor having approximately equal dimensions after etching.